REMARKS

Please reconsider the application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering this application.

Disposition of Claims

Claims 1-18 are pending in this application. By way of this reply, claims 1, 5, 6, 13, 15, and 17 have been amended and claims 4, 14, and 16 have been cancelled without prejudice or disclaimer.

Objection(s)

Claim 3 is objected to regarding the clarity of the phrase "resides on another end of the flip-flop circuit." Per the Examiner's suggestion, claim 3 has been amended to depend from claim 2 rather than claim 1. Accordingly, withdrawal of this objection is respectfully requested.

Rejection(s) under 35 U.S.C § 102

Claims 1-18 stand rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,150,861 ("Matsunaga"). Claims 1 and 13 have been amended in this reply to clarify the present invention recited. Support for these amendments may be found, for example, on pages 16-17 of the Specification. To the extent that this rejection may still apply to the amended claims, the rejection is respectfully traversed.

The present invention relates to an improved flip-flop, which includes embedded

scan logic within the flip-flop logic. As exemplarily shown in Figure 5 of the present application, the flip-flop (80) contains a data input control stage (123) and a scan input control stage (127) on either end. This embedded scan logic allows increased performance relative to flip-flops that have scan circuitry added to flip-flop circuitry rather than embedded scan logic.

Additionally, the present invention uses a mechanism that allows one end of the flip-flop circuit (80) to remain constant while the other end is active. Therefore, while the scan node (SN) is active (*i.e.,* conductive), the data node (DN) is held constant, and vice versa. This allows one end of the flip-flop circuit (80) of the present invention to be skewed or sized to effectuate specific behavior in the flip-flop. Further, the flip-flop circuit (80) of the present invention allows both the data node (DN) and scan node (SN) to be pre-charged high when the PCLK clock signal is low (see Figure 6A where the timing diagram shows both DN and SN high when PCLK is low. This allows less noise and faster propagation of signals when the scan node (SN) or data node (DN) is active.

Matsunaga, in contrast to the present invention, fails to disclose all the limitation of amended independent claims 1 and 13. While Matsunaga discloses a flip-flop circuit (in Figure 2) that contains both a purported scan node (SD or N1) and a purported data node (D or N2), Matsunaga fails to disclose or suggest a mechanism within the flip-flop circuit of Figure 2 that holds one of those nodes constant while the other node is active. Moreover, Matsunaga does not show or suggest a flip-flop circuit that allows for particular nodes to be pre-charged to a certain value and held constant while one end of the flip-flop is active.

Therefore, in view of the above, Matsunaga fails to show or suggest each and

every element of the present invention as recited in the claims as amended. Thus, independent claims 1 and 13, as amended, are patentable over Matsunaga. Dependent claims 2, 3, 5-12, 15, and 17-18 are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.082001).

Respectfully submitted,

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#45,079

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